A Low-Power, Digitally-Controlled, Multi-Stable, CMOS Analog Memory Circuit

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Abstract—This paper presents a digitally-controlled, CMOS analog memory circuit that provides several analog stable operating points based on the laddered inverter quantizer (LIQAF) circuit. Two input digital pulses set the stored analog level by moving the stable operating point up or down through charging or discharging the output node, respectively. The proposed circuit achieves its stable operating levels through nonlinear, continuous-time feedback using only a single supply voltage. We present SPICE simulation results for an 8-level version of the multi-stable circuit in a 65 nm CMOS process. The results demonstrate that the proposed circuit can operate at low-power consumption from a wide range of supply voltages with robust operation across process and temperature variations. The proposed circuit has the potential to be integrated into the grid array of analog neural networks.

Index Terms—Analog circuit, analog neural network, continuous-time feedback, laddered inverter, LIQAF, multi-stable memory, nonlinear, quantizer.

I. INTRODUCTION

The interest in Multi-Stable Memory (MSM) circuit has grown to realize a CMOS-based, multi-bit, analog memory circuit in applications including analog neural networks and fuzzy systems. Various MSM circuits have been reported in the literature [1]–[11]. Analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) are combined to achieve the MSM circuit with indefinite hold time [1], [11]. However, the multiple current branches utilized for the ADC lead to increased current consumption. The capacitor is the simplest form of an MSM circuit, where switches can be used to update the charge on a capacitor [2]. As a capacitor suffers from leakage within the capacitor itself and the circuits connected to it, thereby causing the stored charge to deplete, refresh techniques have been suggested in [5], [6], [12], [13]. These techniques require a clock signal to increase the hold time of the charge on a capacitor, but they involve significant design efforts in maintaining the charge value with low error. In exceptional cases, the leakage can be tolerated such as during the training of Deep Neural Networks (DNNs). Since the weights are updated frequently during the training, recent work by IBM used capacitors to store the weights [3], [4] as shown in Figure 1(a). An MSM circuit is proposed in [7], but it requires multiple reference voltages, as shown in Figure 1(b). A clockless, MSM circuit has been recently proposed in [8]. It stores multiple analog values using a newly introduced circuit called Laddered, Inverter Quantizer (LIQAF) [14], however, it requires an analog input to set the stable output levels.

This paper enhances the authors’ work in [8] by using digital input pulses to control the MSM instead of the analog input. The input digital pulses move up or down the stable operating points of the MSM circuit by simply controlling the pulses’ widths. The all-digital control allows the proposed MSM to be integrated into the grid array design in analog neural networks.

Table I compares the proposed MSM with other approaches, including Static RAM (SRAM) [15] and emerging memory technologies: Resistive RAM (RRAM) [16], [17] and Phase-Change Memory (PCM) [17], [18]. As shown in Table I, the proposed MSM provides CMOS compatibility and high speed, endurance, and retention while supporting analog and multi-bit storage. In addition, the proposed MSM has ultra-low power consumption with < 7 fJ/bit active power at a supply voltage of 1.2 V and with 1.5–500 nW static power at supply voltages of 0.7 V and 1.2 V, respectively.

The main contributions of this paper, compared with [8], can be summarized as follows. First, the proposed MSM has a digital drive circuit that allows an all-digital control compared with the analog control in [8]. Second, we present extensive SPICE simulation results including robustness analysis and DC/transient analysis to verify the circuit operations across a wide range of supply voltages, process and temperature variations, and low power consumption. Finally, we benchmark the proposed MSM against other memory technologies.

The rest of the paper is organized as follows. Section II provides an overview of the LIQAF circuit. Section III presents the proposed MSM circuit. Section IV presents and discusses the simulation results. Finally, conclusions are drawn.

II. LIQAF CIRCUIT DESCRIPTION

To gain an understanding of the LIQAF circuit, consider the simplified structure shown in Figure 2(a), in which only two output levels are implemented [14]. As indicated in Figure 2(b), the circuit can be viewed as a combination of two CMOS inverters that have different ratios of NMOS

![Fig. 1. Previous analog memory circuits: (a) storing charge on a capacitor, (b) utilizing multiple levels with multiple reference voltages.](https://example.com/fig1.png)
TABLE I

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Fig. 2. (a) Basic principles of a two-output LIQAF circuit. (b) Simplified mode (c) Simulated DC characteristics.

versus PMOS gate lengths, thereby yielding the shifted DC characteristics shown in Figure 2(c). When \( V_{in} \) is low and both outputs are high, transistor \( M_1 \) is inactive such that \( V_{out0} \) transitions with increasing \( V_{in} \) according to a CMOS inverter characteristic with one NMOS device, \( M_0 \), and two series PMOS devices, \( M_2 \) and \( M_3 \). In contrast, when \( V_{in} \) is high and both outputs are low, \( M_2 \) is inactive such that \( V_{out1} \) transitions with decreasing \( V_{in} \) according to a CMOS inverter characteristic with two series NMOS, \( M_0 \) and \( M_1 \), devices and one PMOS device, \( M_3 \). Since \( V_{out0} \) cannot transition high unless \( V_{out1} \) is also high, and \( V_{out1} \) cannot transition low unless \( V_{out0} \) is also low, the LIQAF circuit provides guaranteed monotonicity in the quantizer characteristic regardless of the presence of a mismatch. Note that one should not confuse the curves shown in Figure 2(c) with the phenomenon of hysteresis—they instead correspond to the DC characteristic that is independent of the previous state of the input.

### III. PROPOSED DIGITALLY-CONTROLLED MULTI-STABLE MEMORY CIRCUIT

The proposed MSM circuit is a modification of the memory circuit in [8]. To illustrate the proposed MSM, we begin with a 2-level version based on the two-output LIQAF circuit shown in Figure 2. As shown in Figure 3(a), the LIQAF circuit is augmented with a drive circuit and nonlinear feedback attached to each output. Similar to [8], nonlinear feedback is achieved by connecting an NMOS and a PMOS device in series from each LIQAF output to the input, with the gates of these devices being driven by neighboring LIQAF outputs. Since the series NMOS and PMOS devices turn on with a logic 1 and 0 levels, respectively, the LIQAF characteristic is leveraged to enable the appropriate feedback connection to achieve the multi-stable operating point characteristic.

Unlike [8], the proposed MSM is controlled digitally using the drive circuit, which consists of NMOS transistor, \( M_{DP} \), and a PMOS transistor, \( M_{DP} \). Both \( M_{DP} \) and \( M_{DN} \) are controlled by two digital pulses, \( W_{up} \) and \( W_{down} \), respectively. The drive circuit is used to charge or discharge the \( V_{store} \) node to move the stable state up or down. To explain the operation, we assume first that the MSM is settled on \( V_{out0} \) and both \( M_{DN} \) and \( M_{DP} \) are off. Setting \( W_{up} \) to be low for a short time duration turns on \( M_{DP} \) such that \( V_{store} \) is charged-up slightly by the current passing through \( M_{DP} \). The negative feedback will then cause \( V_{store} \) to move the stable operating point one level up, i.e., to \( V_{out1} \). Similarly, if MSM is settled on \( V_{out1} \), setting \( W_{down} \) to be high for a short time duration turns on \( M_{DN} \) such that \( V_{store} \) is discharged slightly by the current passes through \( M_{DN} \). Hence, the negative feedback will then cause \( V_{store} \) to move the stable operating point one level down, i.e. to \( V_{out0} \). To demonstrate the operation of the circuit, Figure 3(b) displays its SPICE simulated transient response, which reveals that two stable operating points are achieved. Further, Figure 3(b) indicates that when both \( M_{DP} \) and \( M_{DN} \) are off, \( V_{store} \) holds the stable operating point indefinitely, without the need for refreshing circuit, as long as the supply voltage is connected to the circuit.

The number of stable operating points of the proposed MSM circuit is increased by using a LIQAF circuit with a higher number of outputs. As shown in Figure 4, eight stable operating points are achieved by using an eight-output LIQAF and correspondingly extending the nonlinear feedback circuit. \( M_{DP} \) and \( M_{DN} \) are sized, based on a 1 ns pulse width of \( W_{up} \) and \( W_{down} \), so that the charge/discharge current moves the stable operating points by one level up or down, respectively. The transistors in the LIQAF and negative feedback are sized to have robust performance across process and temperature shifts.
results confirm the quantization behavior of the LIQAF circuit despite the presence of loading from the nonlinear feedback network.

Figure 6(a) shows the transient waveform of $V_{store}$ for the overall multi-stable circuit shown in Figure 4, at 1.2 V supply voltage and TT at 27°C. Figure 6(a) confirms the operation of the proposed MSM circuit where eight stable operating points are achieved. Besides, both $W_{up}$ and $W_{down}$ have 1 ns pulse width and 100 ns period. SPICE simulation shows a writing speed even lower than 1 ns, thereby confirming the high-speed operation of the proposed circuit. Figure 6(b) and (c) show the simulated transient waveform of $V_{store}$ at FF at 0°C and SS at 70°C, respectively. These figures demonstrate the excellent robustness of the proposed circuit across process and temperature variations.

Figure 7 shows the static power consumption of the proposed MSM circuit during the hold mode at supply voltages of 0.7 V to 1.2 V and TT at 27°C, FF at 0°C, and SS at 70°C process and temperature corners. As indicated in the figure, the proposed circuit has the potential to operate at ultra-low power consumption and low supply voltage. SPICE simulation shows that the energy required to move the stable operating points from the $V_{out0}$ to $V_{out7}$ or vice versa is $\sim$7 femto Joul, thereby translating into energy efficiency of $\sim$7 fJ/bit which enables the proposed circuit to be utilized in applications with extreme constraints on energy, including battery-operated edge devices.

Figure 8 demonstrates the stable operating points of $V_{store}$ for the circuit in Figure 4 at process corners of TT, FF, and SS and temperatures of 27°C, 0°C, and 70°C, respectively.
Although the first and last steps have larger step sizes than the other steps, the proposed circuit achieves overall good linearity and robust performance at different process and temperature variations. Note that calibration techniques can be applied to the proposed MSM circuit to reduce the effect of process and temperature variation.

Figure 9 shows the layout in a 65 nm CMOS process for the 8-level MSM circuit shown in Figure 4. The proposed circuit consumes a total of 8.4 µm x 11.8 µm.

V. CONCLUSIONS

This paper has presented a low-power, digitally-controlled multi-stable analog memory circuit simulated in a 65nm CMOS process. Unlike the prior memory implementation, the proposed circuit can be controlled using digital pulses, thereby easing the integration with standard digital logic systems. Besides, the circuit provides robust performance across process, and temperature variations. Furthermore, the proposed MSM has the potential to be integrated into the grid array designs in analog neural networks.

REFERENCES


